SPECIFICATION AMENDMENTS:

Please amend the Title as follows:

"MULTIBIT SPREAD SPECTRUM ~~SIGNALLING~~ SIGNALING"

Please amend the paragraph beginning at page 4, line 25 as follows:

"The transmitter Tx comprises a ~~HBR~~ high bit rate data source ("HBR") 10 which produces a plurality of symbols in the form of bits at 200kbps. The symbols are supplied by way of a change-over switch SW to a multiplier 12 to which is connected a first code generator ("CG") 14 which supplies an 11 chip PN-code sequence. The 2.2 Mcps output of the multiplier 12 is supplied to a GFSK modulator ("MOD") 16, the output from which is amplified in a power amplifier ("AMP") 18 and propagated by an antenna 20.

A1

Please amend the paragraph beginning at page 5, line 1 as follows:

"A low bit rate ~~(LBR)~~ data source ("LBR") 26 which produces a plurality of symbols in the form of bits at 22.22 kbps is coupled to a multiplier 28 to which is connected a second code generator ("CG") 30 which supplies a 9 chip PN-code sequence. The 200 kcps output from the multiplier 28 is supplied by way of the change-over switch SW, when switched over, to the multiplier 12 in which it is multiplied by the 11 chip PN-code sequence supplied by the first code generator 14 to provide a 2.2 Mcps output. Thereafter the output is processed in the same manner as the spread spectrum HBR signal. In either case the signal propagated by the antenna ~~24~~ 20 is subject to noise."

A2

Please amend the paragraph beginning at page 5, line 10 as follows:

"At the receiver Rx, the propagated signal is received by an antenna 32 and is passed to an RF front end and demodulator ("DEMOD") 34. The output is supplied to a 1 bit analogue-to-digital converter 36 which supplies a 2.2 Mcps signal to a first filter function block ("FFB") 38 to be decoded."

A3

Please amend the paragraph beginning at page 5, line 14 as follows:

"In the filter function block 38 the 2.2 Mcps signal is over-sampled by say a factor of 10. The block 38 has an input 100 for a HBR clock signal, viz. 200kHz, and two outputs, namely, output 102 for signal detect, viz. signal is either below a low threshold, between the low and a high thresholds or above the high threshold, and output 104 for bits out, that is, the higher bit rate decoded bit stream[;]."

A4

Please amend the paragraph beginning at page 5, line 24 as follows:

"The output 104 of the first filter function block 38 comprises a signal at the higher (not oversampled) bit rate which is coupled to an input of a second filter function block ("FFB") 40. The block 40 has an input 200 for a LBR clock signal, viz 22.22 kHz, and two outputs, namely, output 202 for signal detect, which is "1" if a signal is believed to be present but otherwise it is zero and output 204 for bits out, that is, the decoded LBR stream."

A5

Please amend the paragraph beginning at page 6, line 3 as follows:

"Figure 2 illustrates cascaded first and second matched filters 42, 44 for recovering the HBR data, if present, or the LBR data, if present. In the case of the first matched filter 42, it comprises ~~110~~ 11 stage shift register 46 and a ~~110~~ 11 stage register 48 for processing the ten times oversampled chip stream. For convenience of representation each of the stages of the shift register 46 and the register 48 is shown as a macro stage formed by 10 sub-stages. The macro stages of the register 48 stores the 11 chip PN-code sequence. The oversampled chip stream is applied to an input 50 of the shift register 46. Corresponding sub-stages of the registers 46, 48 are coupled to respective XOR gates 52 and their outputs are summed in summing stages 54 to provide a HBR output on a terminal 56. The terminal 56 is connected to a HBR decision stage 58. An output of the stage 58 provides HBR bits or effectively chips at the HBR to the second matched filter 44 which comprises 9 stage shift register 60 and a register 62. The register 60 receives the chips at the high bit rate from the decision stage 58 and the register 62 stores the 9 chips PN-code sequence. XOR gates 64 are coupled to outputs of corresponding stages of the shift register 60 and the register 62.

A6 Cont

AM conct

The outputs of the XOR gates 64 are summed in summing stages 66 which provide a LBR output on a terminal 68. A LBR decision stage 70 is coupled to the terminal 68. The stage 70 makes a hard decision on the LBR bit value which appears on an output 72."

Please amend the paragraph beginning at page 13, line 13 as follows:

AM

"From reading the present disclosure, other modifications will be apparent to persons skilled in the art. Such modifications may involve other features which are already known in the design, manufacture and use of spread spectrum systems and component parts ~~therefor~~ therefore and which may be used instead of or in addition to features already described herein."

Please amend the Abstract as attached hereto.